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AN : 1983-815777 4461

MC : U23-A01B U23-D

PN : DE3313868 A 19831110 DW198346 010pp  
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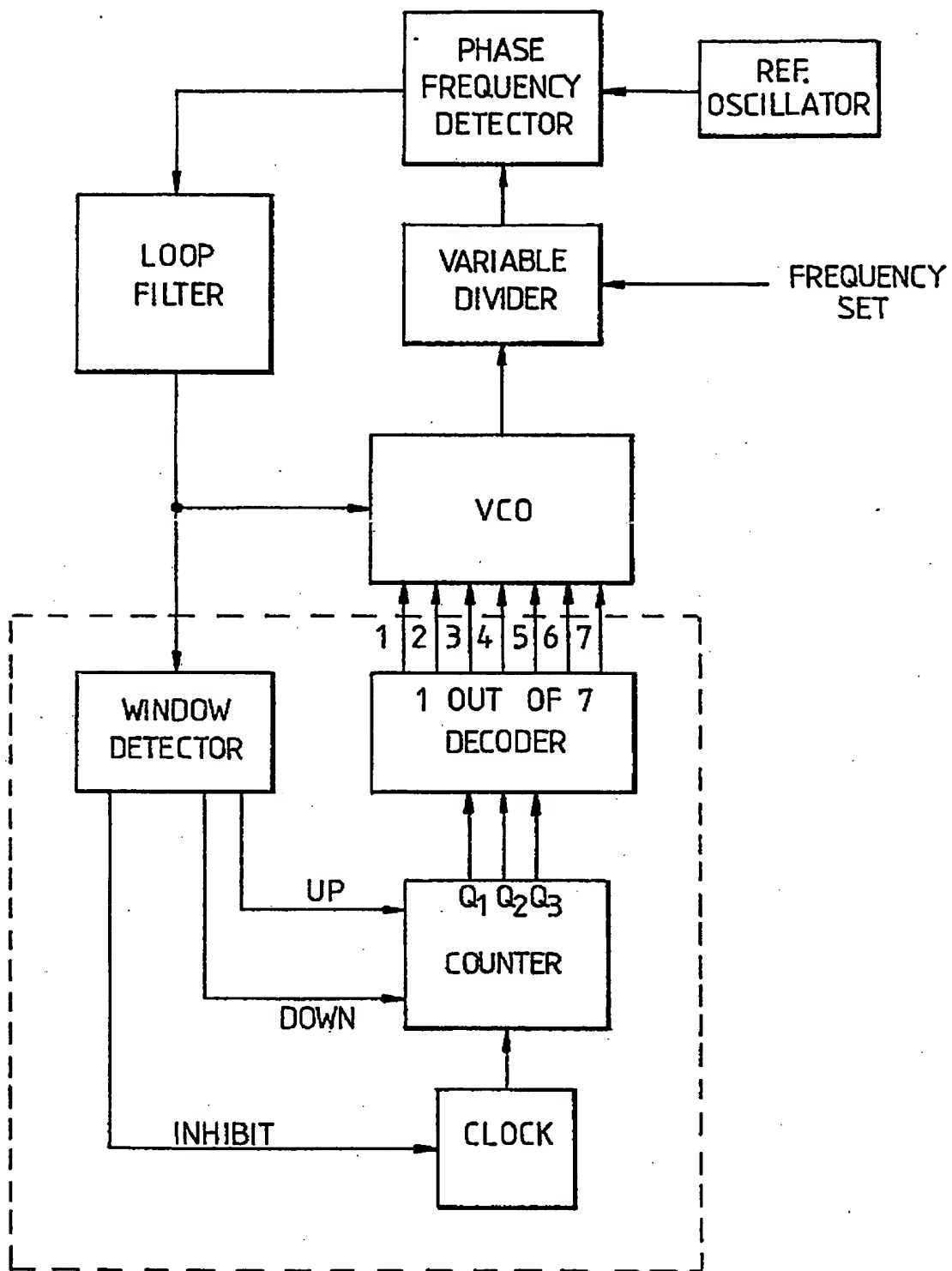
DC : U23

IC : H03L7/08

TI : Wide range VCO with capacitor network - having overlapping frequency ranges and including variable capacitor controlled by regulating voltage from e.g. loop filter output

AB : DE3313868 The oscillator has a wide frequency range which is easily tuned. This is achieved using a window detector which determines the range and generates a range switching signal. A seven stage capacitor network determines the overlapping frequency ranges.  
- A window detector (15) detects the transition from one range to the next by the control voltage and enables a counter (16) controlled by a clock generator (17). The resulting count is decoded by a 1 of 7 decoder (18) which selects the required capacitor.(1/3)

GBAB: GB2120478 A voltage controlled oscillator arrangement which includes an n-stage switchable capacitor network to provide a set of n overlapping VCO frequency ranges and variable capacitance means responsive to a control to adjust the VCO frequency within each frequency range, means for detecting when said control signal exceeds a predetermined upper or lower limit, up/down digital counter means the status of which responds incrementally to output signals from said detecting means, decoding means for decoding the count in the counter means to provide 1-out-of-n range selection signals and switching means responsive to said selection signals to switch said capacitance network.



*Fig. 1*

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(54) **Voltage controlled oscillator**

(57) A wide range voltage controlled oscillator arrangement has a VCO in which an  $n$ -stage switchable capacitor network provides a set of  $n$  overlapping frequency ranges and a variable capacitance responsive to a control signal (e.g. from a feedback loop filter) adjusts the VCO frequency

within each range. A window detector detects when the control signal exceeds upper or lower limits and increments/decrements an up/down counter in association with a clock. The counter contents are applied to a decoder to provide 1-out-of- $n$  range selection signals to effect switching of the VCO capacitor network. Clock is inhibited when the control signal is within the prescribed limits.

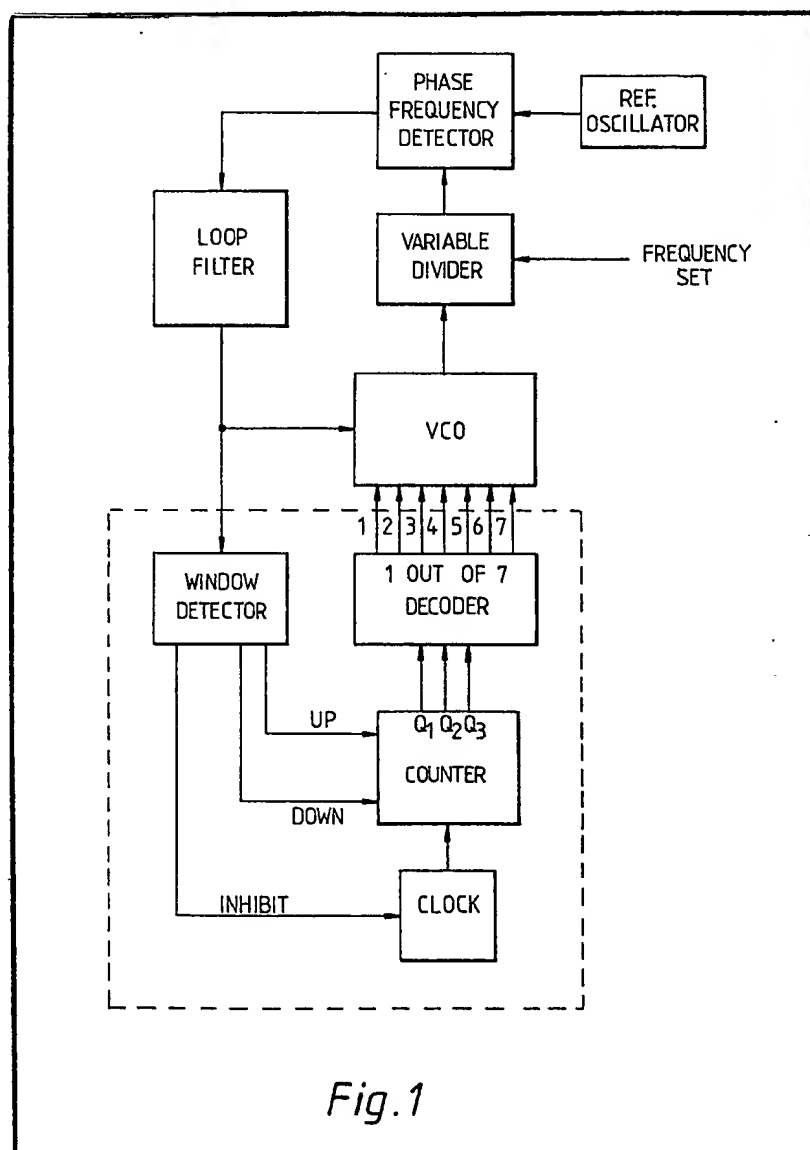
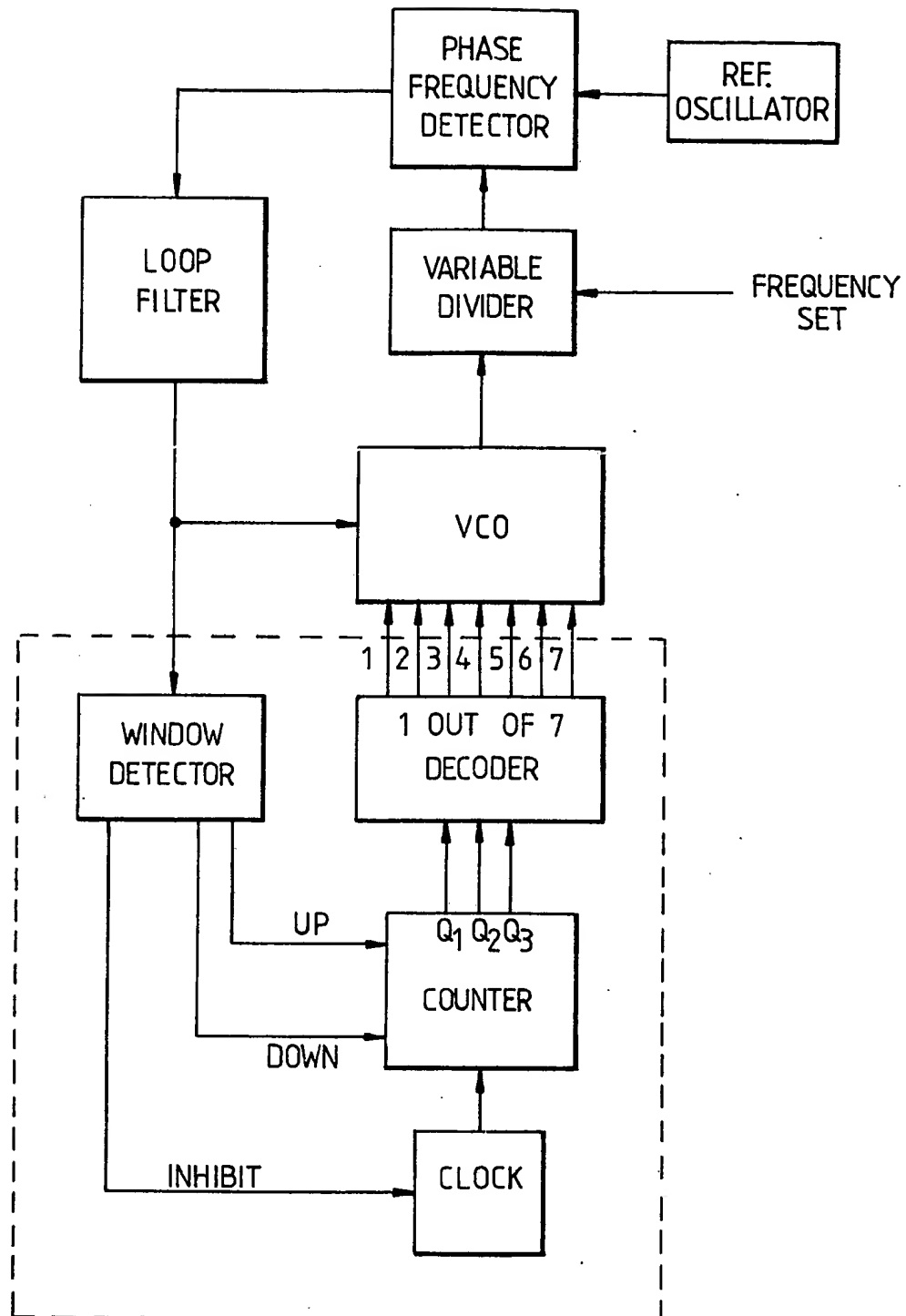


Fig. 1

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$\frac{1}{3}$ *Fig. 1*

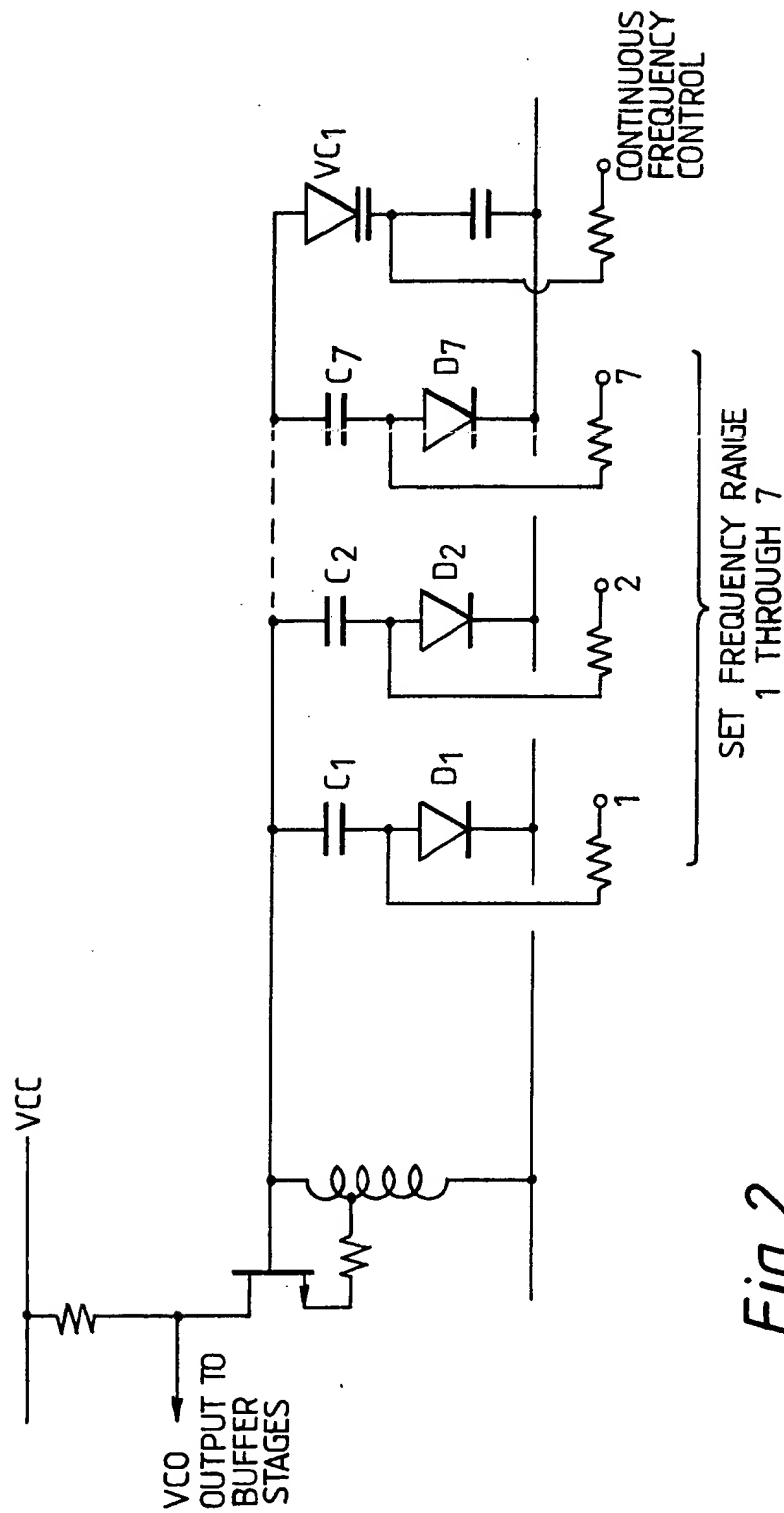
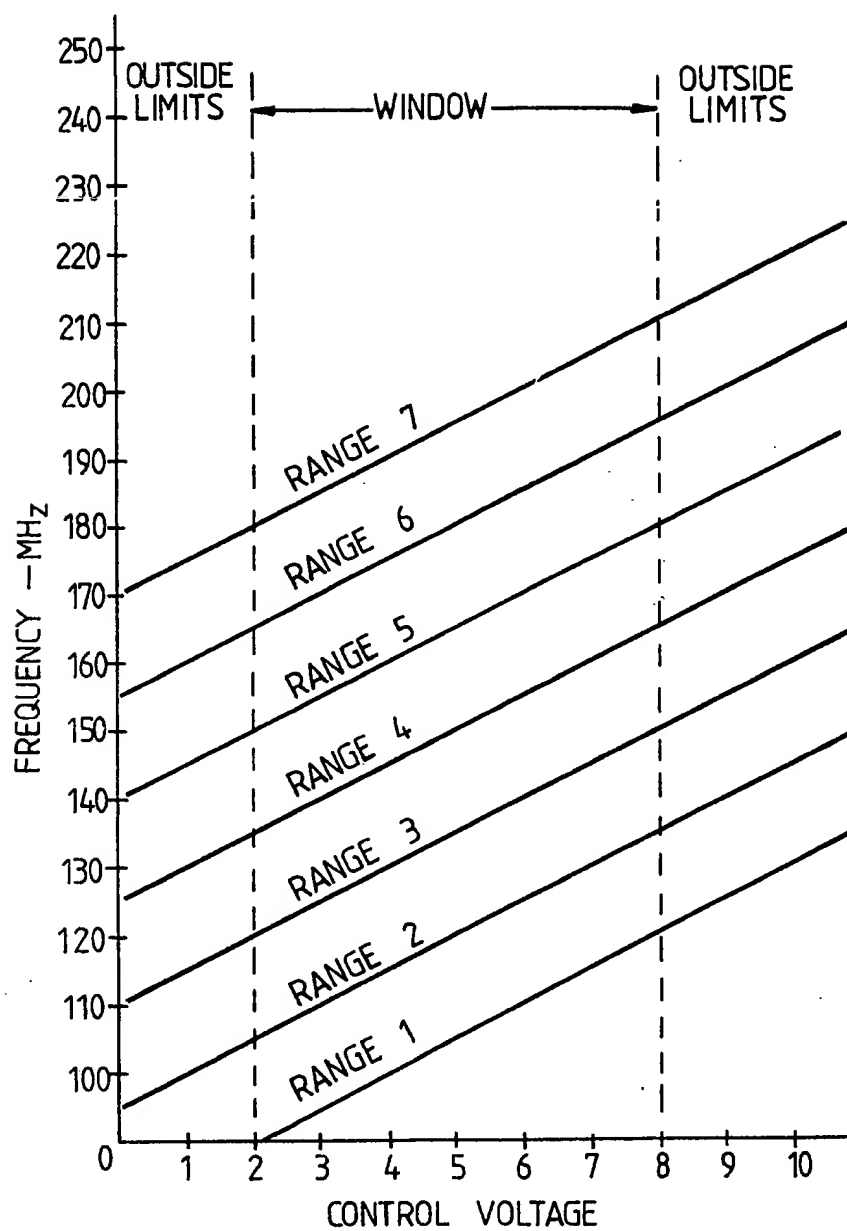


Fig.2

3/3

Fig.3



## SPECIFICATION

## Voltage controlled oscillator

This invention relates to a voltage controlled oscillator, such as may be used in phase locked

5 loop frequency synthesiser.

A common form of phase locked loop frequency synthesiser compares the phase output of a voltage controlled oscillator (VCO) with that of a stable fixed frequency reference oscillator.

10 The difference is fed back, through a loop filter, as a voltage control signal to the VCO. A variable frequency divider inserted in the output of the VCO is used to determine the frequency at which the VCO runs. Thus if the reference oscillator

15 frequency runs at 1 KHz and the divider ratio is 10:1 the VCO output will be 1 MHz.

To achieve a wide frequency range VCO it is known to use a switched capacitor network to provide stepped coarse frequency ranges. Thus in

20 a wide range frequency synthesiser the operator has to set not only the variable divider ratio but also the appropriate VCO frequency range. Fine adjustment of the VCO frequency is then achieved by applying the loop control signal to a variable

25 capacitor within the VCO.

According to the present invention there is

provided a voltage controlled oscillator arrangement which includes an  $n$ -stage

30 switchable capacitor network to provide a set of  $n$  overlapping VCO frequency ranges and variable capacitance means responsive to a control to

adjust the VCO frequency within each frequency range, means for detecting when said control

35 signal exceeds a predetermined upper or lower limit, up/down digital counter means the status of which responds incrementally to output signals

from said detecting means, decoding means for decoding the count in the counter means to

40 provide 1-out-of- $n$  range selection signals and switching means responsive to said selection signals to switch said capacitance network.

An embodiment of the invention will now be described with reference to the accompanying

45 drawings, in which:—

Fig. 1 illustrates in block diagram from a frequency synthesiser incorporating a wide range

VCO,

Fig. 2 illustrates a range setting capacitor

network for the VCO of Fig. 1, and

50 Fig. 3 is a graphical illustration of the operation of the range setting network of Fig. 2.

In the arrangement shown in Fig. 1 the output of voltage controlled oscillator 10 is fed via a

variable divider 11 to a phase frequency detector

12 which also receives a reference frequency

from reference oscillator 13. The detector output

is fed back, via loop filter 14, as a control signal for the VCO. As shown in Fig. 2, the control

voltage for the VCO is determined by a

combination of a switched capacitance network

$C_1, C_2, \dots, C_7$  with a variable capacitance  $VC_1$ . The

variable capacitance effects continuous frequency

control over a limited range and the switched

capacitances provide a series of overlapping

65 ranges within which the continuous frequency control is exercised. Fig. 3 illustrates an idealised set of frequency ranges plotted against variation in VCO control voltage.

The variable capacitor  $VC_1$  in the VCO is a

70 varicap diode and is controlled by the loop filter signal. The loop filter signal is also applied to a "window" detector 15 which determines whether the loop filter output exceeds upper and lower control voltage limits. If the signal exceeds either

75 limit an "up" or "down" signal is sent to a digital 3-stage counter 16. At the same time the window detector removes an inhibit control from a clock circuit 17 so that counter 16 can be

80 incremented or decremented on the next clock pulse. The counter outputs  $Q_1, Q_2, Q_3$  are fed to a 1-out-of-7 decoder 18. The selected decoder output is a voltage which switches the

appropriate capacitor  $C_1, \dots, C_7$  by way of an associated PIN diode  $D_1, \dots, D_7$ . Thus the

85 arrangement shown within the dotted line in Fig. 1 will cause the capacitance network in the VCO to be switched until the loop filter signal settles within the predetermined window, whereafter the

VCO frequency is controlled solely by the variable

90 capacitance. If now the variable divider 11 is set for a new synthesiser output frequency such that the loop filter signal moves out of the window

then the counter and decoder arrangement will

automatically select the correct range within

95 which the new frequency is to be obtained.

## Claims

1. A voltage controlled oscillator arrangement which includes an  $n$ -stage switchable capacitor network to provide a set of  $n$  overlapping VCO

100 frequency ranges and variable capacitance means responsive to a control to adjust the VCO frequency within each frequency range, means for detecting when said control signal exceeds a

predetermined upper or lower limit, up/down

105 digital counter means the status of which responds incrementally to output signals from said detecting means, decoding means for

decoding the count in the counter means to

provide 1-out-of- $n$  range selection signals and

switching means responsive to said selection

110 signals to switch said capacitance network.

2. An oscillator according to claim 1 wherein said switching means comprises a PIN diode in

series with each capacitor, said diodes each being

115 responsive to a respective range selection signal.

3. An oscillator according to claim 1 or 2 wherein said variable capacitance means is a

varicap diode.

4. An oscillator according to any preceding

claim including a source of clock pulses, said

counter means being incremented when said

clock pulses coincide with said output signals

from said detecting means, and means for

inhibiting the application of said clock pulses to

said counter means in the absence of output

125 signals from the detector means.

5. A voltage controlled oscillator arrangement



substantially as described with reference to the  
accompanying drawings.

6. A phase locked loop frequency synthesiser

including a voltage controlled oscillator according  
5 to any preceding claim.

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